The specification has been reviewed and revised to determine and correct all possible minor errors. A Substitute Specification has been submitted to address the Examiner's concerns. No new matter has been added. However, Applicants respectfully disagree with several of the objections made to the specification and submit that the specification, as presented, is clear and concise. Thus, Applicants respectfully request withdrawal of the objections to the specification.

Applicants respectfully submit claims 10 and 17-21 remain unchanged and are presently pending in this application for consideration.

Applicants respectfully submit that the pending claims are patentably distinct over the cited references as required by § 102 and § 103. Applicants further submit that the cited references, whether taken alone or in any combination, fail to disclose the claimed step of forming a logical address/physical address translation table for managing a corresponding relationship between the logical blocks and the physical block areas. Each of the independent claims recites this step or similar language. Thus, these claims are allowable over the cited references. This distinction will be further described in the section that follows.

THE CLAIMS DISTINGUISH OVER THE CITED REFERENCES

As stated in the previous response, a conventional non-volatile memory card includes flash memory cells, such as NOND-type flash memory cells, is divided into physical memory blocks for storing data. The number of physical blocks in a memory card depends on its size. For example, a 16-Mbit NAND-type flash memory card is divided into 512 physical memory blocks, while a 64-Mbit NAND-type flash memory card is divided into 1024 physical memory blocks. On the other hand, data stored in other electronic devices may be arranged in different formats. For instance, a personal computer manages stored data by dividing its storage devices into logical memory blocks. Each of these logical memory blocks is in a different format, such as the size of bits, as compared to the data format of a physical memory block in the memory card. Consequently, when the flash memory card is coupled to a personal computer for data exchange, a logical address/physical address translation table needs to be generated to properly map and transfer data therein between.

The conventional non-volatile memory card typically generates this logical address/physical address translation table during its power-on stage, e.g., when it is inserted into a personal computer. The memory card then stores this translation table in a random access memory (RAM) contained in the memory card. When data are transferred from a logical block of the personal computer to the flash memory card, the data may be stored in any one of the physical memory blocks in the memory card. Thus, the bit-size of physical block addresses in the translation table should be sufficiently large to provide adequate mapping between physical blocks and logical blocks. For instance, 9 bits are required to store the physical block addresses in the translation table for mapping a flash memory card with 512 physical blocks, such as the 16-Mbits flash memory card. A 64-Mbit flash memory card with 1024 physical blocks needs 10 bits to store the physical block addresses in the translation table. Both the 9-bit and the 10-bit addresses respectively require two bytes in the RAM to store them. Thus, the 16-Mbit memory card needs at least 1KB RAM to store the translation table, while the 64-Mbit memory card needs at least 2KB RAM to store the translation table. As the memory size of the flash memory card keeps increasing, a larger size of the RAM in a conventional flash memory card will be necessary. Otherwise, an external RAM will be needed to store this large translation table. The manufacturing costs of the memory card, therefore, will be increased, due to a larger size RAM required therein. See Application, page 1, line 23-page 4, line 35.

The present application describes a method of controlling a memory system that efficiently generates a logical address/physical address translation table stored in the RAM of a flash memory card. According to the present application, when generating the translation table, the method groups two or more physical memory blocks into a physical block area for each corresponding logical block. The address stored in the RAM is inadequate to completely locate the physical block. Rather, the address stored in the RAM specifies the target physical block area and searching identifies which of the blocks stored in the area is correct. Consequently, the described method requires a smaller RAM in the memory card to store the translation table, as compared to the conventional method such as used by AAPA.

FIG. 34 illustrates one embodiment of the present invention where two physical blocks are grouped within a physical block area. In FIG. 34, the logical address/physical address translation table contains the mapping information between the logical blocks and the physical blocks areas. To correctly relate a physical block with a corresponding logical block, a physical block area is first located by looking into the translation table containing the logical block address. After locating the physical block area, the redundant divisions of the tow physical blocks associated with the physical block area are searched to determine which physical block really corresponds to the designated logical block. Accordingly, the presently described method can accurately map the physical blocks with the logical blocks by the translation table. The described method, therefore, effectively reduces the size needed for the RAM to store the translation table. See Application, FIG. 34-35, page 33, line 28-page 35, line 32.

Shinohara discloses a flash memory card with a block memory address arrangement. The flash memory card includes a flash disk control circuit 3, an in-card microprocessor unit (MPU) 4, a logical/physical block address conversion table 5, a flash memory array 6 and a sector buffer 7 including random access memory (RAM). See, Shinohara, col. 4, lines 14-22. Shinohara's invention solves the problems associated with prior art flash memory cards. In these prior art cards, a conversion table exists for each sector for translating logical addresses to physical addresses. Shinohara's invention as well as AAPA is an improvement over the prior art devices in that there exist a conversion table for each block of sectors. However, Shinohara fails to disclose the claimed arrangement of forming a logical address/physical address translation table for managing a corresponding relationship between the logical blocks and the physical block areas. Consequently, Shinohara does not anticipate the pending claims.

In contrast, the Application's method provides in the translation table two levels of address information to identify the location of the targeted physical block. Thus, less address information than is necessary is stored in the translation table to identify the location of the targeted physical block. The final identification of the targeted physical block is accomplished in at least some examples by searching within the physical space of the physical blocks identified by the address of the physical block area.

According to one embodiment of the present invention, in the translation table, logic block 1 corresponds to one of the physical blocks addressed 4 and 5. In this case, the table size is reduced by one bit. In another translation table of another embodiment of the present invention, logic block 1 corresponds to one of the physical blocks addressed 4 to 7. According to this embodiment, the table size is reduced by two bits. The above advantageous feature is never disclosed or suggested by Shinohara or the AAPA.

Claim 10 of the present application recites, in pertinent part, "physical block areas formed by at least two of said physical blocks, the method including preparing a logical address/physical address translation table for managing corresponding relationships between said logical blocks and said physical block areas." As discussed, neither AAPA nor Shinohara describes a mapping of logical addresses to physical that is not one to one (in this case at least two to one). Thus, claim 10 distinguishes over AAPA and Shinohara and is in condition for allowance.

Claim 17 recites, in pertinent part, "forming a table for managing corresponding relationships between said logical blocks and said physical blocks in a random access memory in said system by sequentially preparing required corresponding relationships between said logical blocks and a plurality of physical block areas each including one or more of said physical blocks". As discussed, neither the admitted prior art nor the Hasbun patent describes the definition of an intermediate storage unit (physical block area) that relates logical blocks to physical blocks. Thus, claim 17 distinguishes over AAPA and Shinohara and is in condition for allowance.

Claim 19 recites, in pertinent part, "forming a plurality of areas, each area being formed by an aggregate of at least one of said plurality of physical blocks ... forming an address translation table corresponding to said area in which data in said logical block are stored when said non-volatile semiconductor memory is accessed." Like claim 17 above, claim 19 specifies the definition of an intermediate storage unit (area) that is identified by the address in the translation table. The physical blocks within the area are not identified directly by the translation table. This allows the RAM to be smaller and is not taught by the prior art of record to this application. Applicant submits that claim 19 distinguishes over the art of record and is in condition for allowance.

Claim 20 recites similarly and, in pertinent part, "defining an area formed by one or more of said physical blocks". Applicant submits that claim 20 distinguishes over the art of record and is in condition for allowance.

Claim 21 depends from claim 20. Thus, claim 21 is similarly in condition for allowance.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are required.

CONCLUSION

In view of the foregoing, Applicant respectfully submits that the claims are patentably distinguishable over the cited references as required by 35 U.S.C. §102 and § 103. Throughout the prosecution of this case, Applicants have made an effort to inform the Examiner about the innovative features of the present invention and to advise the Examiner as to how the invention represents a significant advance over the prior art. The nature of the references on which the final rejection rests merely highlights the substantial differences between the claimed invention and the cited references, in structure, the problems solved and how they are solved. Applicants have invented a unique structure that solves many of the problems in existing memory devices. Applicants therefore earnestly request that the Examiner allow this application to pass to issue.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Washington, D.C. telephone number 202 637-3515 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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